Wiznet W5500: A Brief Guide

Version 1.0

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Revision History

Date	Rev	Details
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1. Description

The W5500 chip is a hardwired TCP/IP embedded Ethernet controller that provides easier internet connection to embedded system. It supports TCP, UDP, IPv4, ICMP, ARP, IGMP, and PPPoE protocols. W5500 embeds the 32Kbyte internal memory buffer or the Ethernet packet processing. SPI is provided for easy integration with the external MCU. The SPI interface supports 80 MHz speed and provides two different power modes to reduce power consumption, Wake on LAN (WOL) and power down mode.

2. Features

- Supports Hardwired TCP/IP Protocols: TCP, UDP, ICMP, IPv4, ARP, IGMP, PPPoE.
- Supports 8 independent sockets simultaneously.
- Supports Power down mode.
- Supports Wake on LAN over UDP.
- Supports High Speed Serial Peripheral Interface (SPI MODE 0, 3).
- Internal 32Kbytes Memory for TX/RX Buffers.
- 10BaseT/100BaseTX Ethernet PHY embedded.
- Not supports IP Fragmentation.
- 3.3V operation with 5V I/O signal tolerance.
- LED outputs (Full/Half duplex, Link, Speed, Active).

3. Interface

W5500 provides SPI bus interface with 4 signals (SCSn, SCLK, MOSI, MISO) for external host interfaces, and operates as a SPI slave. There are two modes which SPI interface can be operated on: Variable Length Data mode and Fixed Length Data mode.

At the Variable Length Data mode (Figure 1), it's possible to share the SPI bus with other SPI devices. However, At the Fixed Length Data mode (Figure 2), the SPI bus is dedicate to W5500 and cannot be shared.

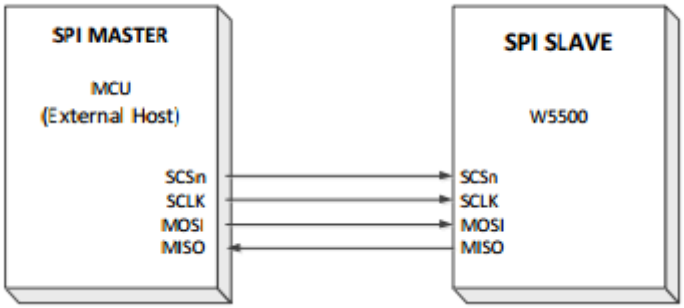

FIGURE 1: VARIABLE LENGTH DATA MODE (SCSN CONTROLLED BY THE HOST)

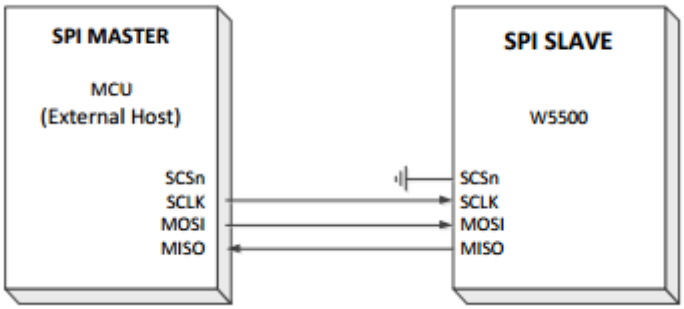

FIGURE 2: FIXED LENGTH DATA MODE (SCSN IS ALWAYS CONNECTED BY GROUND)

The SPI protocol defines four modes for its operation (Mode 0,1,2,3). The W5500 supports SPI Mode 0 and Mode 3. Both MOSI and MISO signals use transfer sequence from Most Significant Bit (MSB) to Least Significant Bit (LSB) .

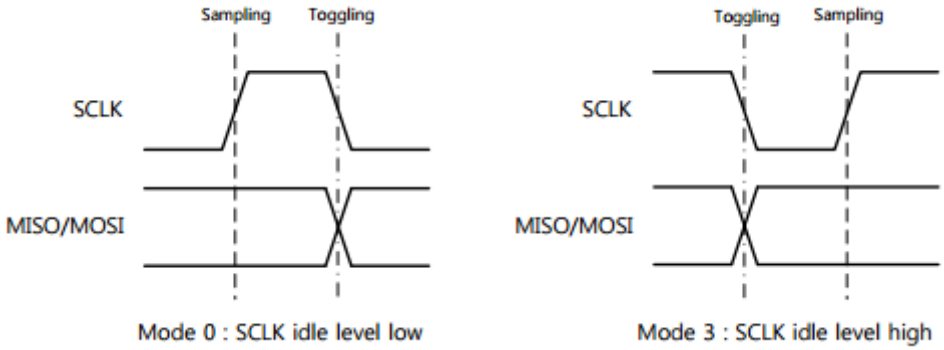

FIGURE 3: SPI MODE 0 & 3

4. SPI Frame

W5500 is controlled by SPI Frame which consists of 16bit Offset Address in Address Phase, 8bits Control Phase and N bytes Data Phase as shown in Figure 4.

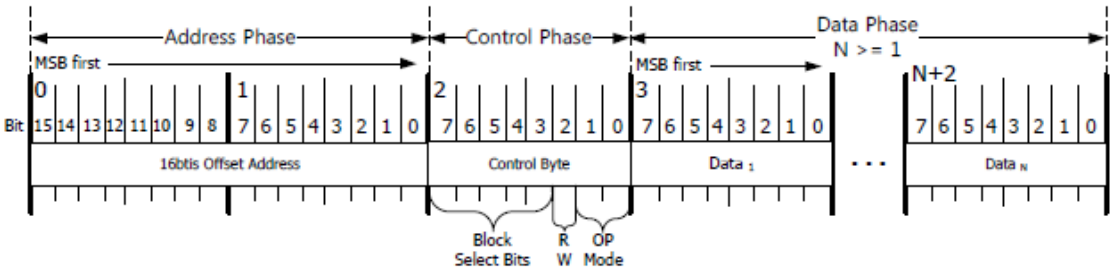

FIGURE 4: SPI FRAME PACKET

4.1. Address Phase

This Address Phase specifies the 16 bits offset address for the W5500 Registers and TX/RX buffer blocks. (From MSB to LSB)

4.2. Control Phase

The Control Phase specifies the block to which the Offset address belongs, the Read/Write Access Mode and the SPI Operation mode.

7	6	5	4	3	2	1	0
BSB4	BSB3	BSB2	BSB1	BSB0	RWB	OM1	OM0

TABLE 1: CONTROL PHASE REGISTER DESCRIPTION

Bit	Symbol	Description
7-3	BSB[4:0]	W5500 has Common Register, 8 Socket Register, TX/RX buffer block for each socket. The next table shows the Block selected by BSB[4:0]

BSB[4:0]	Meaning
00000	Selects Common Register
00001	Selects Socket 0 Register
00010	Selects Socket 0 TX Buffer
00011	Selects Socket 0 RX Buffer
00100	Reserved
00101	Selects Socket 1 Register
00110	Selects Socket 1 TX Buffer
00111	Selects Socket 1 RX Buffer
01000	Reserved
01001	Selects Socket 2 Register
01010	Selects Socket 2 TX Buffer
01011	Selects Socket 2 RX Buffer
01100	Reserved
01101	Selects Socket 3 Register
01110	Selects Socket 3 TX Buffer
01111	Selects Socket 3 RX Buffer
10000	Reserved
10001	Selects Socket 4 Register
10010	Selects Socket 4 TX Buffer
10011	Selects Socket 4 RX Buffer
10100	Reserved
10101	Selects Socket 5 Register
10110	Selects Socket 5 TX Buffer
10111	Selects Socket 5 RX Buffer
11000	Reserved
11001	Selects Socket 6 Register
11010	Selects Socket 6 TX Buffer
11011	Selects Socket 6 RX Buffer

		11100 Reserved 11101 Selects Socket 7 Register 11110 Selects Socket 7 TX Buffer 11111 Selects Socket 7 RX Buffer
2	RWB	**Read/Write Access Mode Bit** The sets Read/Write Access Mode '0' : Read '1' : Write
1-0	OM[1:0]	SPI Operation Mode Bits This sets the SPI operation mode. Either variable Length Data or Fixed Length Data - Variable Length Data Mode (VDM): Data Length is controlled by SCSn. External Host makes SCSn Signal Assert (High-to-Low) and informs the start of the SPI Frame Address Phase to W5500. Then the external host transfers the Control Phase with **OM[1:0]="00".** After N-Bytes Data Phase transfers, SCSn Signal is De-asserted (Low-to-High) and informs the end of the SPI Frame Data Phase to W5500.

4.3. Data Phase

When the Control Phase set by the SPI Operation Mode Bits OM[1:0] = "00". The Data Phase is set to the N-Byte length (VDM mode).

5. Common Register Block

Common Register Block configures the general information of W5500 such as IP and MAC address.

TABLE 2: OFFSET ADDRESS FOR COMMON REGISTER

Offset	Register	Offset	Register	Offset	Register
0x0000	Mode (MR)	0x0013	Interrupt Low Level Timer (INTLEVEL0)	0x0021	(PHAR3)
		0x0014	(INTLEVEL1)	0x0022	(PHAR4)
				0x0023	(PHAR5)
0x0001	Gateway Address (GAR0)				
0x0002	(GAR1)	0x0015	Interrupt (IR)	0x0024	PPP Session Identification (PSID0)
0x0003	(GAR2)			0x0025	(PSID1)
0x0004	(GAR3)	0x0016	Interrupt Mask (IMR)		
				0x0026	PPP Maximum Segment Size (PMRU0)
0x0005	Subnet Mask Address (SUBR0)	0x0017	Socket Interrupt (SIR)	0x0027	(PMRU1)
0x0006	(SUBR1)				
0x0007	(SUBR2)	0x0018	Socket Interrupt Mask (SIMR)	0x0028	Unreachable IP address (UIPR0)
0x0008	(SUBR3)			0x0029	(UIPR1)
		0x0019	Retry Time (RTR0)	0x002A	(UIPR2)
0x0009	Source Hardware Address (SHAR0)	0x001A	(RTR1)	0x002B	(UIPR3)
0x000A	(SHAR1)				
0x000B	(SHAR2)	0x001B	Retry Count (RCR)	0x002C	Unreachable Port (UPORTR0)
0x000C	(SHAR3)			0x002D	(UPORTR1)
0x000D	(SHAR4)	0x001C	PPP LCP Request Timer (PTIMER)		
0x000E	(SHAR5)			0x002E	PHY Configuration (PHYCFGR)
		0x001D	PPP LCP Magic number (PMAGIC)	0x002F	
0x000F	Source IP Address (SIPR0)			-	Reserved
0x0010	(SIPR1)	0x001E	PPP Destination MAC Address (PHAR0)	0x0038	
0x0011	(SIPR2)	0x001F	(PHAR1)		
0x0012	(SIPR3)	0x0020	(PHAR2)	0x0039	Chip version (VERSIONR)
0x003A - 0xFFFF		Reserved			

6. Socket Register Block

W5500 supports 8 Sockets for communication channel. Each socket is controlled by Socket n Register Block (when 0<n<7). The n value of Socket n Register can be selected by BSB[4:0] of SPI Frame.

TABLE 3: OFFSET ADDRESS IN SOCKET N REGISTER BLOCK

Offset	Register	Offset	Register	Offset	Register
0x0000	Socket n Mode (Sn_MR)	0x0010 0x0011	Socket n Destination Port (Sn_DPORT0) (Sn_DPORT1)	0x0024 0x0025	Socket n TX Write Pointer (Sn_TX_WR0) (Sn_TX_WR1)
0x0001	Socket n Command (Sn_CR)				
0x0002	Socket n Interrupt (Sn_IR)	0x0012 0x0013	Socket n Maximum Segment Size (Sn_MSSR0) (Sn_MSSR1)	0x0026 0x0027	Socket n RX Received Size (Sn_RX_RSR0) (Sn_RX_RSR1)
0x0003	Socket n Status (Sn_SR)	0x0014	Reserved	0x0028 0x0029	Socket n RX Read Pointer (Sn_RX_RD0) (Sn_RX_RD1)
0x0004 0x0005	Socket n Source Port (Sn_PORT0) (Sn_PORT1)	0x0015	Socket n IP TOS (Sn_TOS)		
		0x0016	Socket n IP TTL (Sn_TTL)	0x002A 0x002B	Socket n RX Write Pointer (Sn_RX_WR0) (Sn_RX_WR1)
0x0006 0x0007 0x0008 0x0009 0x000A 0x000B	Socket n Destination Hardware Address (Sn_DHAR0) (Sn_DHAR1) (Sn_DHAR2) (Sn_DHAR3) (Sn_DHAR4) (Sn_DHAR5)	0x0017 - 0x001D	Reserved	0x002C	Socket n Interrupt Mask (Sn_IMR)
		0x001E	Socket n Receive Buffer Size (Sn_RXBUF_SIZE)	0x002D 0x002E	Socket n Fragment Offset in IP header (Sn_FRAG0) (Sn_FRAG1)
		0x001F	Socket n Transmit Buffer Size (Sn_TXBUF_SIZE)	0x002F	Keep alive timer (Sn_KPALVTR)
0x000C 0x000D 0x000E 0x000F	Socket n Destination IP Address (Sn_DIPR0) (Sn_DIPR1) (Sn_DIPR2) (Sn_DIPR3)	0x0020 0x0021	Socket n TX Free Size (Sn_TX_FSR0) (Sn_TX_FSR1)	0x0030 - 0xFFFF	Reserved
		0x0022 0x0023	Socket n TX Read Pointer (Sn_TX_RD0) (Sn_TX_RD1)		

7. Register Descriptions

This section contains a description of the registers which are going to be used in implementing the Ethernet driver. Check datasheet (1) for the reference of any missing registers.

7.1. Common Registers

- **MR (Mode Register):** MR is used for S/W reset, ping block mode and PPPoE mode.

7	6	5	4	3	2	1	0
RST	Reserved	WOL	PB	PPPoE	Reserved	FARP	Reserved

Check W5500 Datasheet (Page 32) for details.

- **GAR (Gateway IP Address Register):** GAR configures the default gateway address.
  Ex) in case of "192.168.0.1"

0x0001	0x0002	0x0003	0x0004
192 (0xC0)	168 (0xA8)	0 (0x00)	1 (0x01)

- **SUBR (Subnet Mask Register):** SUBR configures the subnet mask address
- **SIPR (Source IP Address Register)**: SIPR configures the source IP address
- **IR (Interrupt Register):** IR indicates the interrupt status. Each bit of IR will be still "1" until the bit will be written to '1' by the host. If IR is not equal to '0x00', INTn PIN is asserted low until it is '0x00'

7	6	5	4	3	2	1	0
CONFLICT	UNREACH	PPPoE	MP	Reserved	Reserved	Reserved	Reserved

Bit	Symbol	Description
7	CONFLICT	**IP Conflict** Bit is set as „1" when own source IP address is same with the sender IP address in the received ARP request.
6	UNREACH	**Destination unreachable** When receiving the ICMP (Destination port unreachable) packet, this bit is set as '1'. When this bit is '1', Destination Information such as IP address and Port number may be checked with the corresponding UIPR & UPORTR.
5	PPPoE	**PPPoE Connection Close** When PPPoE is disconnected during PPPoE mode, this bit is set
4	MP	**Magic Packet** When WOL mode is enabled and receives the magic packet over UDP, this bit is set.

- **IMR (Interrupt Mask Register):** IMR is used to mask interrupts. Each bit of IMR corresponds to each bit of IR. So, when a bit of IMR is '1' and the corresponding bit of IR is '1', an interrupt will be issued. Otherwise, it will be neglected.

- **SIR (Socket Interrupt Register)**: SIR indicates the interrupt status of Socket. Each bit of SIR be still '1' until Sn_IR is cleared by the host. If Sn_IR is not equal to '0x00', the n-th bit of SIR is '1' and INTn PIN is asserted until SIR is '0x00'
- **SIMR (Socket Interrupt Mask Register):** SIMR is used as mask interrupts for SIR. It works the same as IMR.
- **RTR (Retry Time-Value Register):** RTR configures the retransmission timeout period. The unit of timeout period is 100us and the default of RTR is '0x07D0' or '2000' (200us).
  Example when timeout-period is set as 400ms, RTR = (400ms / 1ms) X 10 = 4000(0x0FA0)

0x0019	0x001A
0x0F	0xA0

- **RCR (Retry Count Register):** RCR configures the number of time of retransmission. When retransmission occurs as many as 'RCR+1', Timeout interrupt is issued (Sn_IR[TIMEOUT] = '1')
- **PHAR (Destination Hardware Address Register in PPPoE mode):** PHAR should be written to the PPPoE server hardware address acquired in PPPoE connection process.
- **UIPR (Unreachable IP Address Register) and UPORTR (Unreachable Port Register):** W5500 receives an ICMP packet(Destination port unreachable) when data is sent to a port number which socket is not open and UNREACH bit of IR becomes '1' and UIPR & UPORTR indicates the destination IP address & port number respectively.

7.2. Socket Registers

- **Sn³_MR (Socket n Mode Register):** Sn_MR configures the option or protocol type of Socket n.

7	6	5	4	3	2	1	0
MUTLI/MFEN	BCASTB	ND/MC/MMB	UCASTB MIP6B	P3	P2	P1	P0

- **Sn_CR (Socket n Command Register) :** This register is used to set the command for Socket n such as OPEN, CLOSE, CONNECT. After W5500 accepts the command, the Sn_CR register is automatically cleared to 0x00

Value	Symbol
0x01	OPEN
0x02	LISTEN
0x04	CONNECT
0x08	DISCON
0x10	CLOSE
0x20	SEND
0x21	SEND_MAC
0x22	SEND_KEEP
0x40	RECV

- **Sn_IR (Socket n Interrupt Register):** This register indicates the status of Socket interrupt such as establishment, termination, receiving data, timeout). To clear the Sn_IR bit, the host should write the bit to '1'.

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	SEND_OK	TIMEOUT	RECV	DISCON	CON

- **Sn_IMR (Socket n Interrupt Mask Register):** Sn_IMR masks the interrupt of Socket n.
- **Sn_SR (Socket n Status Register):** Sn_SR indicates the status of Socket n. the status of Socket n is changed by Sn_CR or some special control packet as SYN, FIN Packet in TCP.
  (Check datasheet for more details - Page 49-50)
- **Sn_PORT (Socket n Source Port Register):** Sn_PORT configures the source port number of Socket n. It is valid when Socket n is used in TCP/UPD mode. It should be set before OPEN command is ordered.
- **Sn_DHAR (Socket n Destination Hardware Address Register):** This register configures the destination hardware address of Socket n when using SEND_MAC command in UDP mode or it indicates that it is acquired in ARP-process by CONNECT/SEND command.
- **Sn_DIPR (Socket n Destination IP Address Register):** Sn_DIPR configures or indicates the destination IP address of Socket n. It is valid when Socket n is used in TCP/UDP mode.
  In TCP client mode, it configures an IP address of 'TCP server' before CONNECT command.
  In TCP server mode, it indicates an IP address of 'TCP client' after successfully establishing connection.
  In UDP mode, it configures an IP address of peer to be received the UDP packet by SEND or SEND_MAC command.
- **Sn_DPORT (Socket n Destination Port Register):** Sn_DPORT configures or indicates the destination port number of Socket n. It works the same as Sn_DIPR register.
- **Sn_MSSR (Socket n Maximum Segment Size Register):** This register configures the maximum transfer unit (MTU) of Socket n.

Mode	Normal (MR(PPPoE) = '0')		PPPoE (MR(PPPoE)='1')	
	Default MTU	Range	Default MTU	Range
TCP	1460	1 - 1460	1452	1 - 1452
UDP	1472	1 - 1472	1464	1 - 1464
MACRAW	1514			

- **Sn_TTL (Socket n TTL Register):** Sn_TTL configures the TTL (Time To Live field in IP header) of socket n.
- **Sn_RXBUF_SIZE (Socket n RX Buffer Size Register):** Sn_RXBUF_SIZE configures the RX buffer block size of Socket n. Socket n RX Buffer Block size can be configured with 1,2,4,8, and 16 Kbytes. If a different size is configured, the data cannot be normally received from a peer.

Value (dec)	0	1	2	4	8	16
Buffer Size	0KB	1KB	2KB	4KB	8KB	16KB

- **Sn_TXBUF_SIZE (Socket n TX Buffer Size Register):** it configures the TX buffer block size of Socket n. It's configured the same way as Sn_RXBUF_SIZE register

- **Sn_TX_FSR (Socket n TX Free Size Register):** Sn_TX_FSR indicates the free size of Socket n TX Buffer Block. It is initialized to the configured size by Sn_TXBUF_SIZE. Data bigger than Sn_TX_FSR should not be saved in the Socket n TX Buffer because the bigger data overwrites the previous saved data not yet sent. Therefore, check before saving the data to the Socket n TX Buffer, and if data is equal or smaller than its checked size, transmit the data with SEND/SEND_MAC command after saving the data in Socket n TX buffer. But, if data is bigger than its checked size, transmit the data after dividing into the checked size and saving in the Socket n TX buffer.
- **Sn_TX_RD (Socket n TX Read Pointer Register):**
  Sn_TX_RD is initialized by OPEN command. However, if Sn_MR(P[3:0]) is TCP mode('0001'), it is re-initialized while connecting with TCP. After its initialization, it is auto-increased by SEND command. SEND command transmits the saved data from the current Sn_TX_RD to the Sn_TX_WR in the Socket n TX Buffer.
- **Sn_TX_WR (Socket n TX Write Pointer Register) :**
  Sn_TX_WR is initialized by OPEN command. However, if Sn_MR(P[3:0]) is TCP mode('0001'), it is re-initialized while connecting with TCP.
  It should be read or to be updated like as follows.
  1. Read the starting address for saving the transmitting data.
  2. Save the transmitting data from the starting address of Socket n TX buffer.
  3. After saving the transmitting data, update Sn_TX_WR to the increased value as many as transmitting data size. If the increment value exceeds the maximum value oxFFFF (greater than ox10000 and the carry bit occurs), then the carry bit is ignored and will automatically update with the lower 16bits value.
  4. Transmit the saved data in Socket n TX Buffer by using SEND/SEND command

- **Sn_RX_RSR (Socket n Received Size Register):** This register indicates the data size received and saved in Socket n RX Buffer. It's calculated as the difference between Sn_RX_WR and Sn_RX_RD.
- **Sn_RX_RD (Socket n RX Read Data Pointer Register):** Sn_RX_RD is initialized by OPEN command. Make sure to be read or updated as follows.
  1. Read the starting save address of the received data.
  2. Read data from the starting address of Socket n RX Buffer.
  3. After reading the received data, Update Sn_RX_RD to the increased value as many as the reading size. If the increment value exceeds the maximum value oxFFFF, that is, is greater than ox10000 and the carry bit occurs, update with the lower 16bits value ignored the carry bit.
  4. Order RECV command is for notifying the updated Sn_RX_RD to W5500.

- **Sn_RX_WR (Socket n RX Write Pointer Register):** This register is initialized by OPEN command and it is auto-increased by the data reception.

8. Electrical Specifications

8.1. DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	Apply VDD, AVDD	2.97	3.3	3.63	V
V_{IH}	High level input voltage		2.0		5.5	V
V_{IL}	Low level input voltage		-0.3		0.8	V
I_{DD1}	Supply Current (Normal Operation Mode)	VDD = 3.3V, AVDD=3.3V, T=25C		132		mA
I_{DD2}	Supply Current (Power Down Mode)	PHY Power Down mode, VDD=3.3V, AVDD=3.3V, T=25C		13		mA
I_{OH}	High level output current	VOH = 2.4V, All outputs except XO	12.5	26.9	47.1	mA
I_{OL}	Low level output current	VOL = 0.4V, All outputs except XO	8.6	13.9	18.9	mA

8.2. Power Dissipation

Condition	Min	Typ	Max	Unit
100M Link	-	128	-	mA
10M Link	-	75	-	mA
Un-Link	-	65	-	mA
100M Transmitting	-	132	-	mA
10M Transmitting	-	79	-	mA
Power Down mode	-	13	-	mA

9. Reference

1. WizNet 5500 Datasheet.
http://www.mouser.com/pdfdocs/w5500_ds_v100e.PDF