SPI Protocol

Version 1.0

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Revision History

Date	Rev	Details
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1. Definition

SPI (Serial Peripheral Interface) is a de facto standard protocol originally developed by Motorola, well suited for on-board communications between integrated circuits. The protocol is synchronous, can work in full duplex, and does not need addressing to differentiate between devices on the bus, which allows higher transfer rates ranging up to several megabits per second. SPI can achieve much higher data transfer rates than I2C, but requires much more wiring. SPI, to overcome the lack of addressing, requires a select line for each slave. SPI's simplicity of application and high data rates make it very suitable for single master, single slave applications. However, it can be troublesome for applications with several slaves, due to the complexity of wiring. Single-master and multi-master configuration are possible with SPI, however, SPI does not specify how multi-master should be implemented and it is rarely used and awkward. SPI is being incorporated in various integrated circuits, such as ADCs, DACs, flash memories and SD cards.

2. Interface

An SPI interface uses four signals:

1. SCLK (Serial clock): Used for clocking, controls the flow of data on the MOSI and MISO lines. This signal is driven by the master owning the bus.
2. MOSI (Master Out, Slave In): Used to transfer data from a master to a slave.
3. MISO (Master In, Slave Out): Used to transfer data from a slave to a master.
4. SS (Slave Select): Used to activate/select a slave, each slave requires its own SS wire.

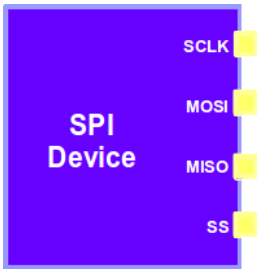

FIGURE 1: SPI INTERFACE

Term	Description
Transmitter	A device that send data through the bus
Receiver	A device that receives data through the bus
Master	A device that initiates and terminates data exchange sessions, and generates clock signals
Slave	A device addressed by a master
Multi-master	More than one master connected to the bus

TABLE 1: TERMS DEFINITIONS

3. Mechanism

The SPI bus consists of four signal lines: SCLK, MOSI, MISO and SS. The SCLK, MOSI and MISO are shared by all devices on the bus (see figure 1). On the other hand, each slave has its own SS line connecting it with its master. Communications on the bus are always initiated by a master by triggering a SS signal (usually active low), and only one master can own the bus at a time. The SS signal should be kept active until the end of each exchange session. In single slave configurations, the SS signal can be kept always low, however, some devices require the falling edge of the SS signal to initiate communications.

Upon each communication, the master initiating the communication configures the clock, which determines the transfer rate on MOSI and MISO. Note that the frequency of the clock should be equal to or less than the maximum frequency the slave supports. The SPI bus allows the master and the slave to send and receive data at the same time (full duplex), but not all SPI devices support or need this. There are no rules that specify how to access the data, nor the width of data packets exchanged on the bus. Each SPI device could require its own set of rules.

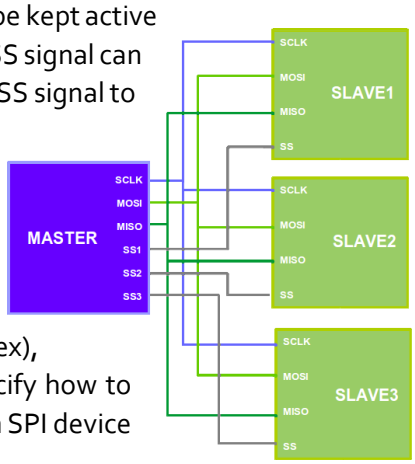

FIGURE 2: SPI BUS STRUCTURE

4. Clock Polarity and Phase

Data sampling and transfer rate are controlled by the clock. SPI devices sample data on the rising edge of the clock, and propagate data on the falling edge, or vice versa. Different devices use different timing, the engineer should look up this on the datasheet. The clock polarity (CPOL) and the clock phase (CPHA) specify the timing of data sampling and propagation. The CPOL determines the base value of the SCLK line. If the CPOL = 0, this means that the SCLK is 0 when there is no communication on the bus (i.e. when the bus is idle). Table 2 shows the different settings for CPOL and CPHA, and figure 2 depicts the timing for each configuration.

Mode	CPOL	CPHA	Timing
0	0	0	Data are sampled on the rising edge of the clock, and propagated on the falling edge.
1	0	1	Data are sampled on the falling edge of clock, and propagated on the rising edge of the clock.
2	1	0	Data are sampled on the falling edge of the clock, and propagated on the rising edge of the clock.
3	1	1	Data are sampled on the rising edge of the clock, and propagated on the falling edge.

TABLE 2: CPOL AND CPHA SETTINGS

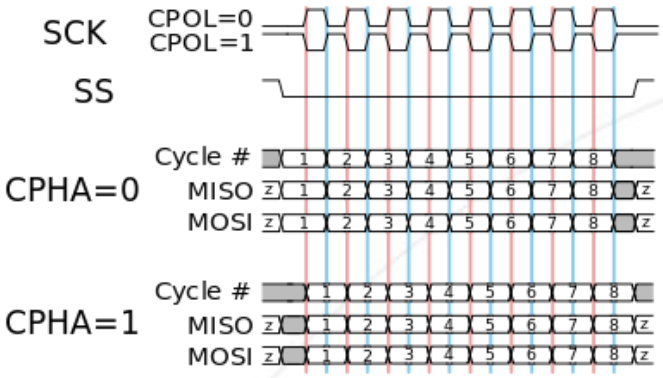

FIGURE 3: SPI BUS TIMING

5. Data Exchange

For any data exchange on the bus, the following steps should be followed:

1. The master configures the clock's frequency, polarity, and phase.
2. The master issues a SS signal to a slave.
3. The master and the slave exchange data on the MOSI and MISO lines.
4. The master ends the session by deactivating the SS signal.

Normally, the master and the slave, each has a shift register to buffer exchanged data.